(Declared u/s 3 of UGC Act, 1956)

Department of Electronics and Communication Engineering

Sub Code/Name: **BEC4L1- ELECTRONIC CIRCUIT DESIGN LAB**

Name : ……

Reg No : ……

Branch : ……

Year & Semester : ……

LIST OF EXPERIMENTS

INDEX

S.no	Name of the Experiment	Marks	Staff SIGN

Ex No:1(a)

Date:

FEEDBACK AMPLIFIER

(CURRENT-SERIES FEEDBACK AMPLIFIER)

Aim:

To design and test the current-series feedback amplifier and to calculate the following parameters with and without feedback.

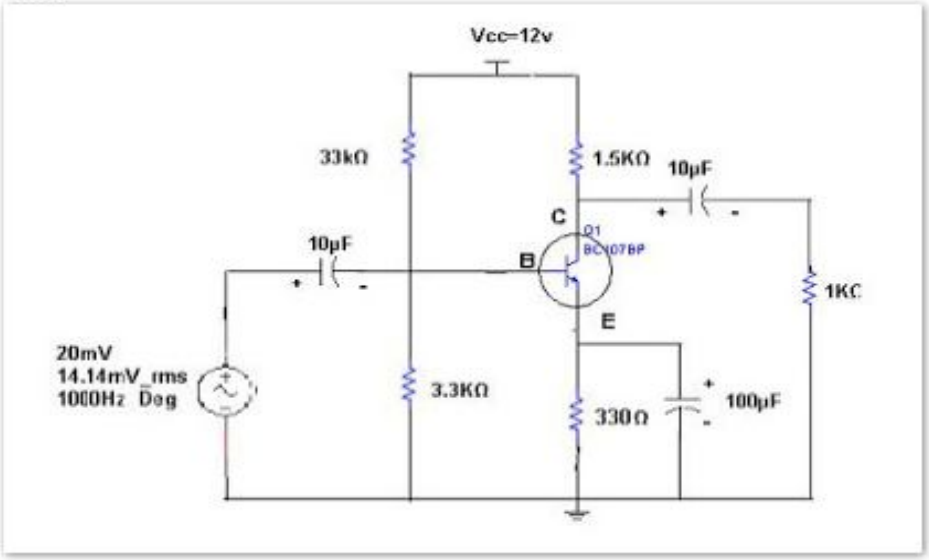
1. Mid band gain.
2. Bandwidth and cut-off frequencies.
3. Input and output impedance.

Components & Equipment required:

S.NO	APPARATUS	RANGE	QUANTITY
1.	Power supply	(0-30)V	1
2.	Function generator	(0-1M)Hz	1
3.	CRO	(0-20)MHz	1
4.	Transistor	BC107	1
5.	Resistors	330Ω,1 KΩ,1.5 KΩ,,3.3 KΩ,33KΩ	Each 1
6.	Capacitors	10 µF,100µF	Each 1
7.	Connecting wires	-	Bunch
8	Bread board	-	1

Theory: The current series feedback amplifier is characterized by having shunt sampling and series mixing. In amplifiers, there is a sampling network, which samples the output and gives to the feedback network. The feedback signal is mixed with input signal by either shunt or series mixing technique. Due to shunt sampling the output resistance increases by a factor of 'D' and the input resistance is also increased by the same factor due to series mixing. This is basically transconductance amplifier. Its input is voltage which is amplified as current.

CIRCUIT DIAGRAM:



Procedure:

1. Connections are made as per circuit diagram.
2. Keep the input voltage constant at 20mV peak-peak and 1kHz freq cy.For different values of load resistance, note down the output voltage and calculate the gain by using the expression

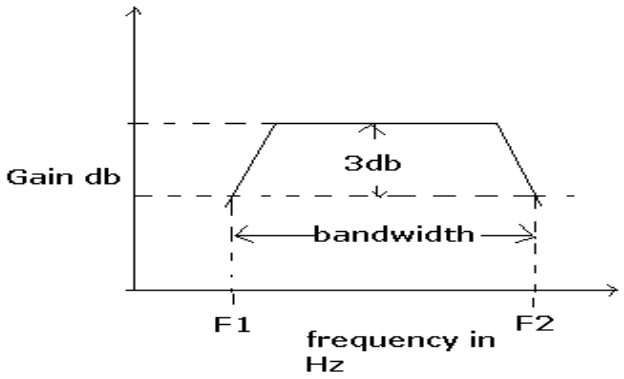
$$A_v = 20\log(V_0 / V_i)\ dB$$

3. Remove the emitter bypass capacitor and repeat STEP 2.And observe the effect of feedback on the gain of the amplifier.
4. For plotting the frquency the input voltage is kept constant at 20mV peak-peak and the frequency is varied from 100Hz to 1MHz.
5. Note down the value of output voltage for each frequency. All the readings are tabulated and the voltage gain in dB is calculated by using expression $A_v = 20\log (V_0 / V_i)\ dB$
6. A graph is drawn by takung frquency on X-axis and gain on Y-axis on semi log graph sheet
7. The Bandwidth of the amplifier is calculated from the graph using the expression Bandwidth B.W = $f_2 - f_1$.

Tabulation:

Sl No	Frequency(Hz)	Output(Vo)(Volts)	Gain(A)=Vo/Vi	Gain in dB=20log(Vo/Vi)

Model graph:



Result: Thus the current series feedback amplifier was designed and constructed and the following parameters are calculated.

a) Frequency in ……..Hz
b) Gain in…….dB
c) Bandwidth f_H-f_L .....……Hz

VIVA QUESTIONS:

1. What is feedbackamplifier?

Thepart ofthe output isgiven to theinput of thecircuitcalledasfeedbackamplifier.

2. Classify the feedbackamplifiers.

1) Voltage seriesfeedbackamplifier

2) Current series feedbackamplifier

3) Voltageshunt feedbackamplifier

4) Current shunt feedbackamplifier

3. What is meant byneutralization?

Itistheprocessbywhichfeedbackcanbecancelledbyintroducingacurrentthatisequalinmagnitudebut180^{o}outofphasewiththefeedbacksignalattheinputoftheactivedevice.Thetwosignalswillcancelandtheeffectoffeedbackwillbeeliminated.Thistechnique is termedasneutralization.

4. **What is the applicationoftunedamplifiers?**

Theapplicationoftunedamplifierstoobtainadesiredfrequwnctandrejectingallotherfrequencyin

(i).Radio and T.V broadcastingas tunning circuit.(ii). Wirelesscommunicationsystem

Ex No:1(b)

Date:

DESIGN AND ANALYSIS OF VOLTAGE SHUNT FEEDBACK AMPLIFIER

Aim:

To design and test the voltage-shunt feedback amplifier and to calculate the following parameters with and without feedback.

1. Mid band gain.
2. Bandwidth and cut-off frequencies.
3. Input and output impedance.

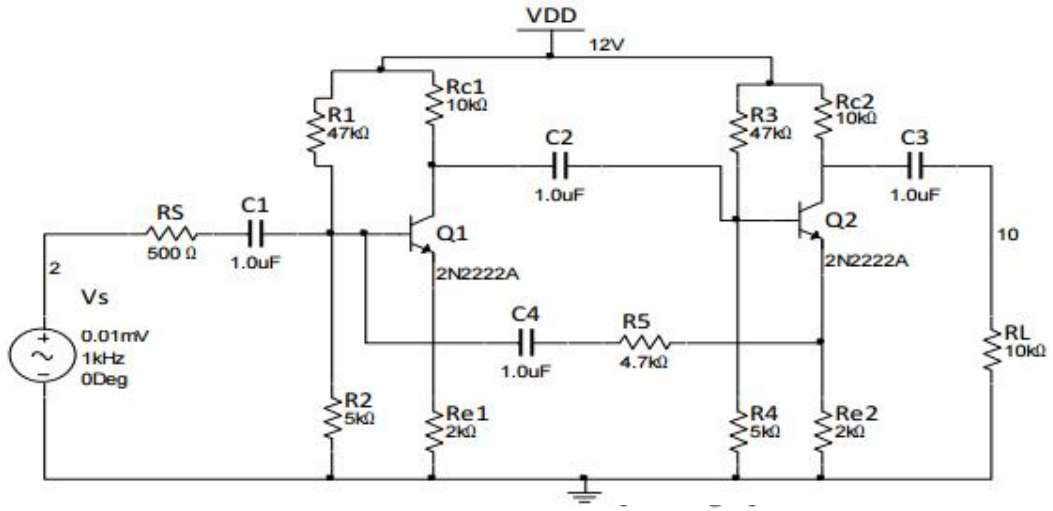
Components & Equipment required:

S.NO	APPARATUS	RANGE	QUANTITY
1.	Power supply	(0-30)V	1
2.	Function generator	(0-1M)Hz	1
3.	CRO	(0-20)MHz	1
4.	Transistor	2N2222A	1
5.	Resistors	10 KΩ,47 KΩ, 4.7 KΩ ,500 Ω,2 KΩ,5KΩ	3,2,1,1,2,2
6.	Capacitors	1.0 μF	4
7.	Connecting wires	-	Bunch
8	Bread board	-	1

Theory:

In voltage shunt feedback amplifier, the feedback signal voltage is given to the base of the transistor in shunt through the base resistor RB. This shunt connection tends to decrease the input resistance and the voltage feedback tends to decrease the output resistance. In the circuit RB appears directly across the input base terminal and output collector terminal. A part of output is feedback to input through RB and increase in IC decreases IB. Thus negative feedback exists in the circuit. So this circuit is also called voltage feedback bias circuit. This feedback amplifier is known a transresistance amplifier. It amplifies the input current to required voltage levels. The feedback path consists of a resistor and a capacitor.

CIRCUIT DIAGRAM:



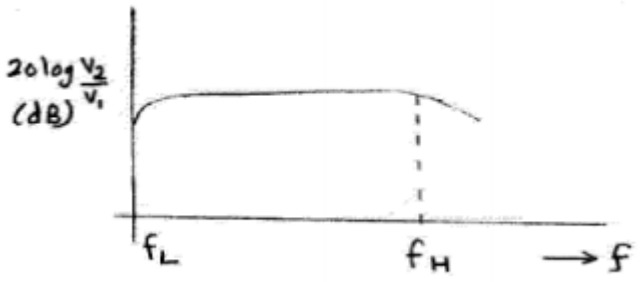
PROCEDURE: -

1. Connect the circuit diagram as shown in figure. Adjust input signal amplitude 50mV, 1 KHz in the function generator and observe an amplified voltage at the output without distortion.
2. By keeping input signal voltage, constant 50mV, vary the input signal frequency from 1 to 1MHz in steps as shown in tabular column and note the corresponding output voltages. By keeping feed- back terminals open and calculate the Bandwidth from the graph.
3. Connect the Feedback short A and B terminal and now vary the input signal frequency from 1 to 1MHz in steps as shown in tabular column and note the corresponding output voltage
4. Calculate the Bandwidth with feed- back from the plot of graph.

Tabulation:

Sl No	Frequency(Hz)	Output(Vo)(Volts)	Gain(A)=Vo/Vi	Gain in dB=20log(Vo/Vi)

Model graph:



Result: Thus the Voltage shunt feedback amplifier was designed and constructed and the following parameters are calculated.

a) Frequency in ……..Hz
b) Gain in…….dB
c) Bandwidth f_H-f_L ……Hz

VIVA QUESTIONS:

1. Give an example for voltage-series feedback.

The Common collector or Emitter follower amplifier is an example for voltage series feedback.

2.Give the properties of negative feedback.

i. Negative feedback reduces the gain
ii. Distortion is very much reduced

3. Define voltage shunt feedback.

A fraction of output voltage is supplied in parallel with the input voltage through the feedback network. The feedback signal is proportional to the output voltage

4.Define voltage series feedback.

The input to the feedback network is in parallel with the output of the amplifier. A fraction of the output voltage through the feedback network is applied in series with the input voltage of the amplifier.

5.Define current shunt feedback.

The shunt connection at the input reduce the input resistance and the series connection at the output increase the output resistance is called current shunt feedback

Ex No:2
Date:

TRANSISTOR PHASE SHIFT OSCILLATOR

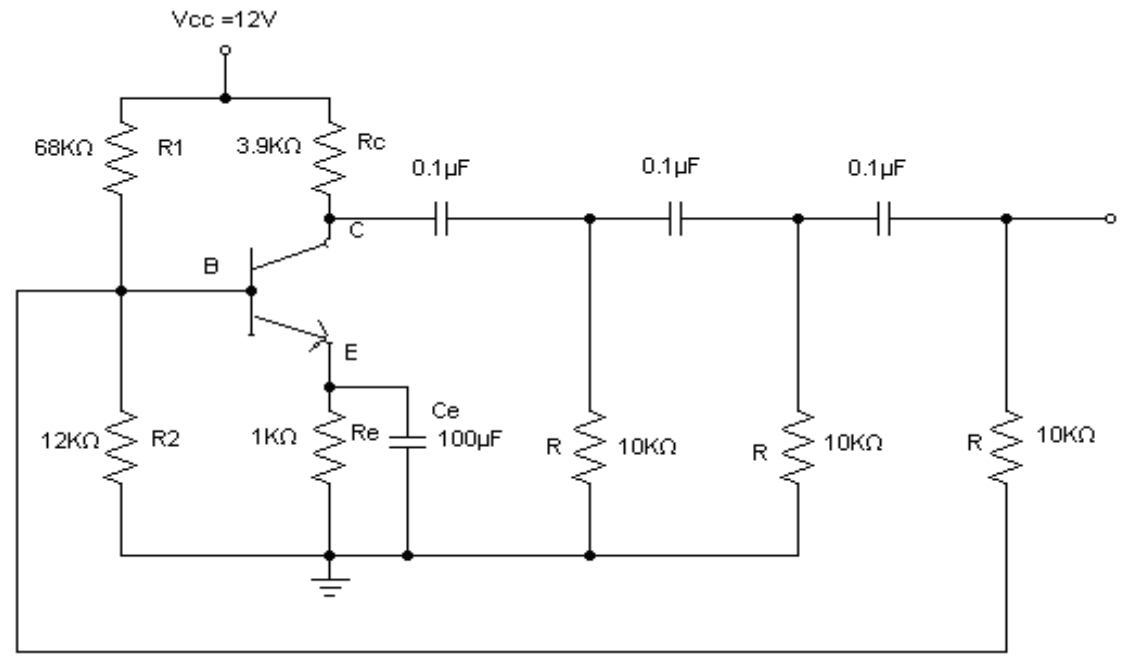
Aim: To design and construct a RC phase shift oscillator for the given frequency (f_0).

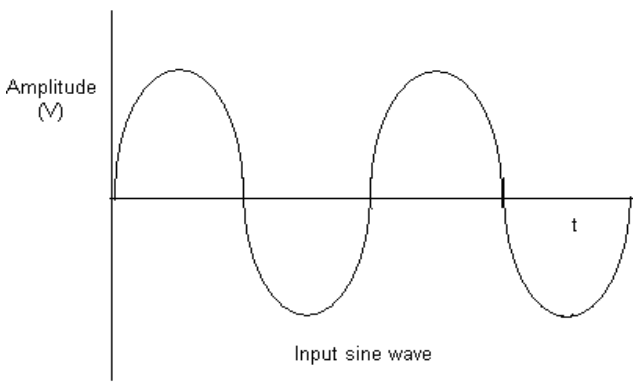
Components & Equipment required:

S.NO	APPARATUS	RANGE	QUANTITY
1.	Power supply	(0-30)V	1
2.	Function generator	(0-1)MHz	1
3.	CRO	(0-20)MHz	1
4.	Transistor	BC107	1
5.	Resistors	1 kΩ,68 kΩ,3.9 kΩ,12KΩ,10kΩ	1,1,1,1,3
6.	Capacitors	0.1µF,100 µF	
7.	Connecting wires	-	Bunch

Theory: In the RC phase shift oscillator, the required phase shift of 180˚ in the feedback loop from the output to input is obtained by using R and C components, instead of tank circuit. Here a common emitter amplifier is used in forward path followed by three sections of RC phase network in the reverse path with the output of the last section being returned to the input of the amplifier. The phase shift Φ is given by each RC section $\Phi=\tan^{-1}(1/\omega rc)$. In practice R-value is adjusted such that Φ becomes 60˚. If the value of R and C are chosen such that the given frequency for the phase shift of each RC section is 60˚. Therefore at a specific frequency the total phase shift from base to transistor's around circuit and back to base is exactly 360˚ or 0˚. Thus the Barkhausen criterion for oscillation is satisfied

Circuit diagram:





Procedure:

1. Connections are made as per the circuit diagram.
2. Switch on the power supply and observe the output on the CRO (sine wave).
3. Note down the practical frequency and compare with its theoretical frequency.

TABULAR COLUMN:

Amplitude(Volts)	Time(ms)	Frequency(KHz)

Result: Thus RC phase shift oscillator is designed and constructed and the output sine wave frequency is calculated as

VIVA QUESTIONS:

1. What is Oscillator circuit?

A circuit with an active device is used to produce an alternating current is called an oscillator circuit.

2.What are the different types of oscillators?

1. sinusoidal oscillator 2, Relaxation oscillator 3. Negative resistance oscillator 4. Feedback oscillator 5. LC oscillator 6. RC Phase shift oscillator.

3. What are the conditions for oscillations?

The magnitude of loop gain must be unity. Total phase shift around closed loop is zero.

4.Define frequency oscillation.

When the signal level increases, the gain of the amplifier is decrease at a particular value of output, the gain of the amplifier is reduced exactly equal to 1/β then the output voltage remain constant at frequency is called frequency oscillation.

5. What is the application of RF phase shift oscillator?

It is used for amplification, phase shifting and oscillation.

Ex No:3

Date:

SINGLE TUNED CLASS A AMPLIFIER

Aim: To plot the frequency response of a single tuned class A amplifier.

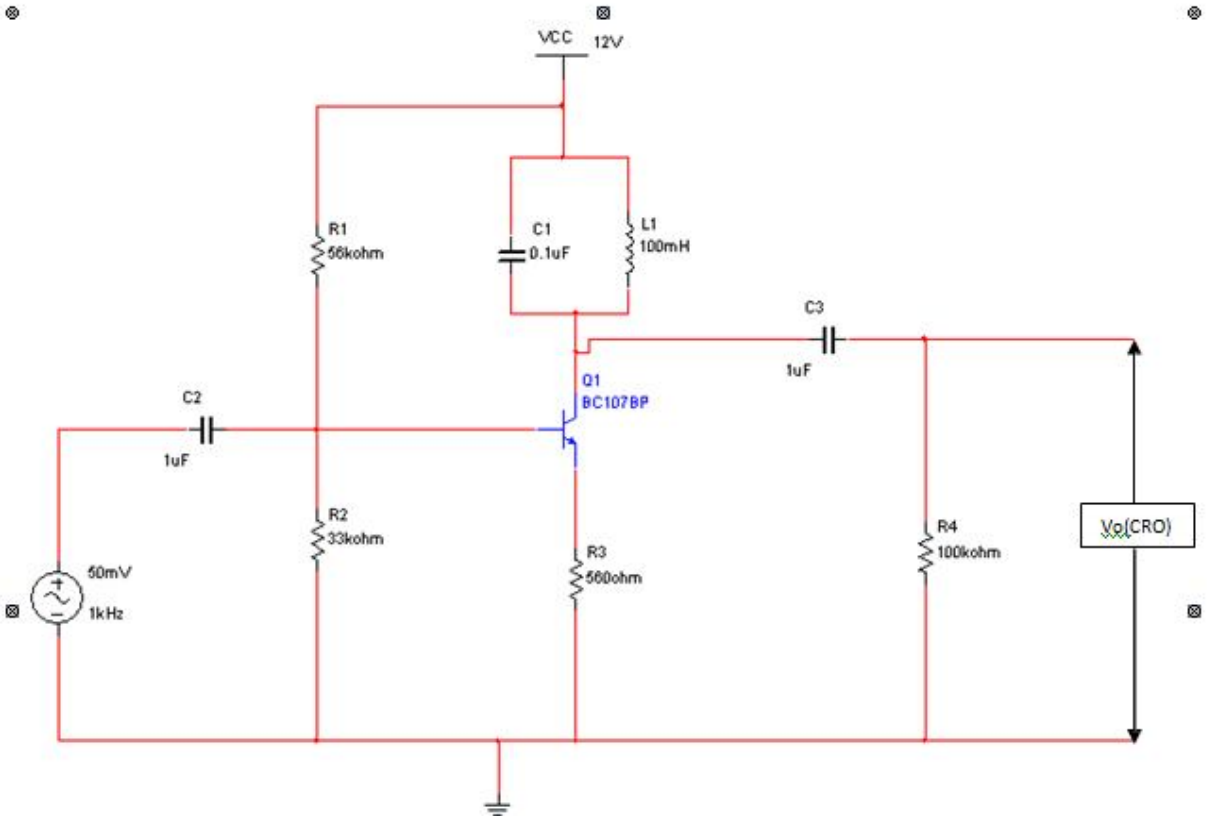
APPARATUS :

Apparatus	Range	Quantity
Transistor	BC107	-1 No
Resistors	33 kΩ	-1 No
	56 kΩ	-1 No
	100 kΩ	-1 No
	560 Ω	-1 No
capacitor	1µF,0.1 µF	-2 No,1 No
Inductor	100mH,	-1 No
CRO	Dual channel(0-20MHz)	-1 No
Function generator	(1Hz-1MHz)	-1 No
RPS	(0-30V)	-1 No
Breadboard	-	-1 No
Connecting wires	-	-1 No

THEORY:

The signal to be amplified and it is applied between the terminals base and emitter . The tank circuit(i.eL&R) is located at collector terminal and it may be varied in such a way that the resonant frequency becomes equal to the frequency of the input signa l . At resonant the tuned circuit offers high impedance and thus given input signal is amplified and thus appears with large value across it and other frequencies will be rejected. The response of the tuned amplifiers falls sharply below and above the resonant frequency. So the tuned circuit selects the desired frequency and rejects all other frequencies.

CIRCUITDIAGRAM:



Procedure:

1. Connections are to be made as per the circuit diagram on bread board properly.

2. Set input signal v_i=50mVusingthe Signal Generator.

3. Keep the input voltage constant and varythefrequencyfrom10 Hz to 100kHzin steps as shown in the tabular column and note the output voltage.

4. Plot the graph of voltage gain in dB V_S frequency.

5. Calculate the bandwidth from the graph.

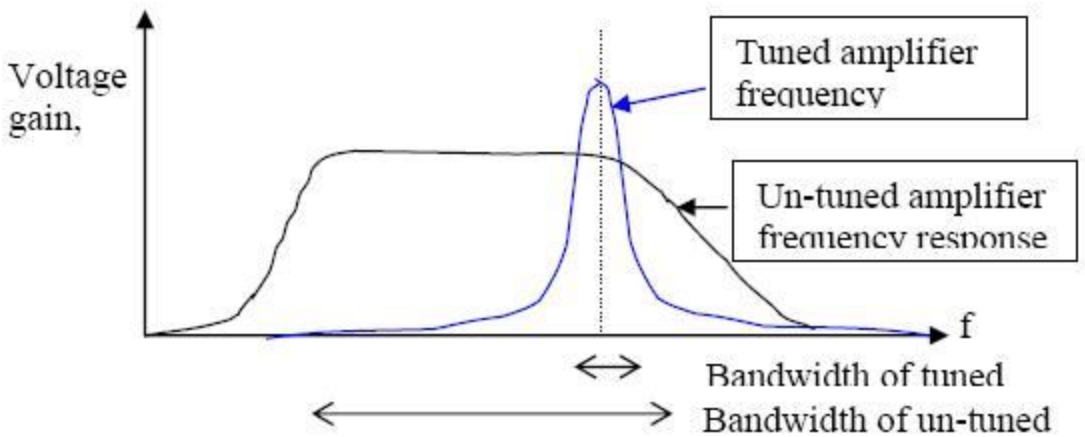
OBSERVATIONS

Tabular form:

frequency	Gain=(V_o/V_i)	Gain in dB= 20log(gain)
10Hz		
100Hz		
500Hz		
1kHz		
1.2khz		
1.22kHz		
1.24kHz		
1.26kHz		
1.28kHz		
1.30kHz		
1.32kHz		
1.34kHz		
.36kHz		
1.38kHz		
1.40kHz		
1.42kHz		
1.44kHz		
1.46kHz		
1.5kHz		
2kHz		
10kHz		
100kHz		

(the values for the above designed circuit will be obtained from 1.2 or 1.30KHzto 1.40KHz.before or after this values the output will not be seen .)

Frequencyresponse:



THEORITICALCALCULATIONS:

L=100mH ,C=0.1μF

$f_o=1/2\pi\sqrt{(LC)}$

RESULT:

Thus the frequencyresponseof single tuned voltageamplifierhas been studied and its bandwidthhasbeencalculated.

Ex No:4(a)

Date:

LC OSCILLATORS

AIM:

To design a Colpitts oscillator and to observe its output waveform.

a) APPARATUS REQUIRED :

S.NO	APPARATUS	SPECIFICATION	QUANTITY
1.	Transistor	BC 107	1
2.	Resistors	31.14 KΩ, 1.2KΩ,150KΩ,300Ω	Each 1
3.	Capacitors	0.1 µF,10 µF,100µF	1, 2,1
4.	Inductor	2.79mH	1
5.	RPS	±12V	1
6.	CRO	1MHz	1
7.	Connectingwires	-	Req.

b) DESIGN PROCEDURE:

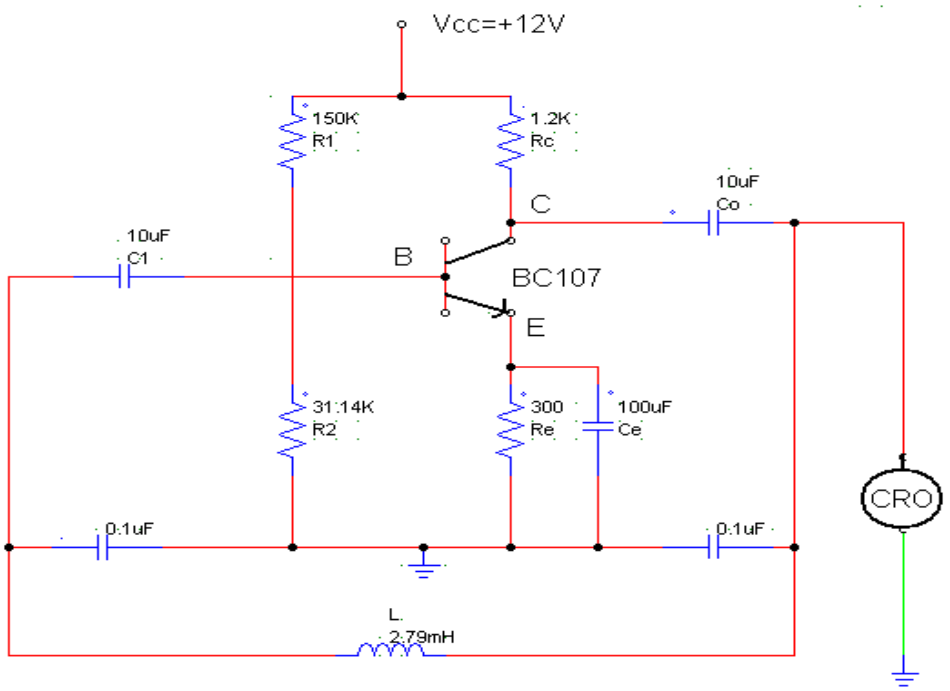
Select a appropriate transistor and note down its specification such as V_{CE},$I_{C(MAX)}$,$h_{fe(min)}$and $V_{be(sat)}$.

- $V_{CC}= V_{CEQ}$
- $R_2=S* R_E$
- $V_{CC}[R_2/(R_1+ R_2)=V_{BE}+V_{BE(SAT)}$
- $V_{R1}+V_{R2}=V_{CC}$
- $h_{fe} \geq C_1* C_2/(C_1+ C_1)$
- $X_{CE} \leq R_E/10$

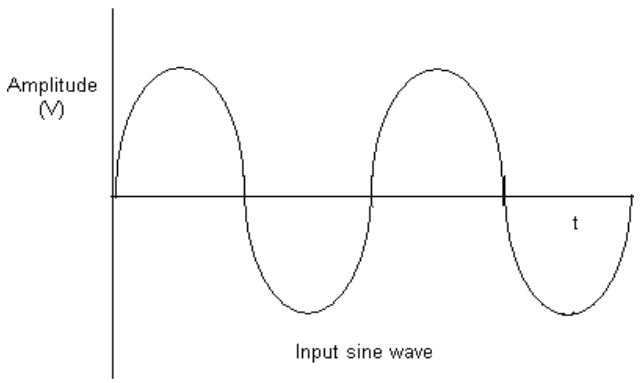
PROCEDURE:

- Hook up the circuit as shown in the circuit diagram.
- Switch on the power supply.
- Slight modification in value of $C_1$and C_2can bemadeto get perfect sine wave output.
- Observe the output waveform in CRO.

c) CIRCUITDIAGRAM:COLPITTS OSCILLATOR



d) MODELGRAPH:



e) TABULATION:

Amplitude(Volts)	Time(ms)	Frequency(KHz)

f) RESULT:

Thus the Colpitts oscillator was designed and its output waveform was verified.

VIVA QUESTIONS:

1. What is piezoelectric effect?

The piezo electric Crystals exhibit a property that if a mechanical stress is applied across one face the electric potential is developed across opposite face. The inverse is also live.This phenomenon is called piezo electric effect.

2. List the disadvantagesofcrystalOscillator.

It is suitableforonlylowpowercircuits

Largeamplitude of vibrations maycrackthecrystal.

Itlargeinfrequencyisonlypossiblereplacingthecrystalwithanotheronebydifferentfrequency.

3. What are parasiticOscillators?

Ina practical amplifier circuit dueto straycapacitancesand lead inductances,oscillationsresult, sincethe circuitconditions satisfythe Barkhavsen's criterion.TheseOscillatorsarecalledasunwanted orparasitic Oscillations

4. What is damped Oscillation?

TheelectricalOscillationsinwhichtheamplitudedecreaseswithtimearecalledasdampedOscillation.

Ex No:4(b)

Date:

LC OSCILLATORS

AIM:

To design a Hartley oscillator and to observe its output waveform.

APPARATUS REQUIRED:

S.NO	APPARATUS	SPECIFICATION	QUANTITY
1.	Transistor	BC 107	1
2.	Resistors	31.14 KΩ, 300 Ω,1.2KΩ,150KΩ	Each 1
3.	Capacitors	0.007µF,10µF, 100µF	1,2,1
4.	Inductor	200mH	2
5.	RPS	±12V	1
6.	CRO	1MHz	1
7.	Connectingwires	-	Req.

DESIGN PROCEDURE:

Select a appropriate transistor and note down its specification such

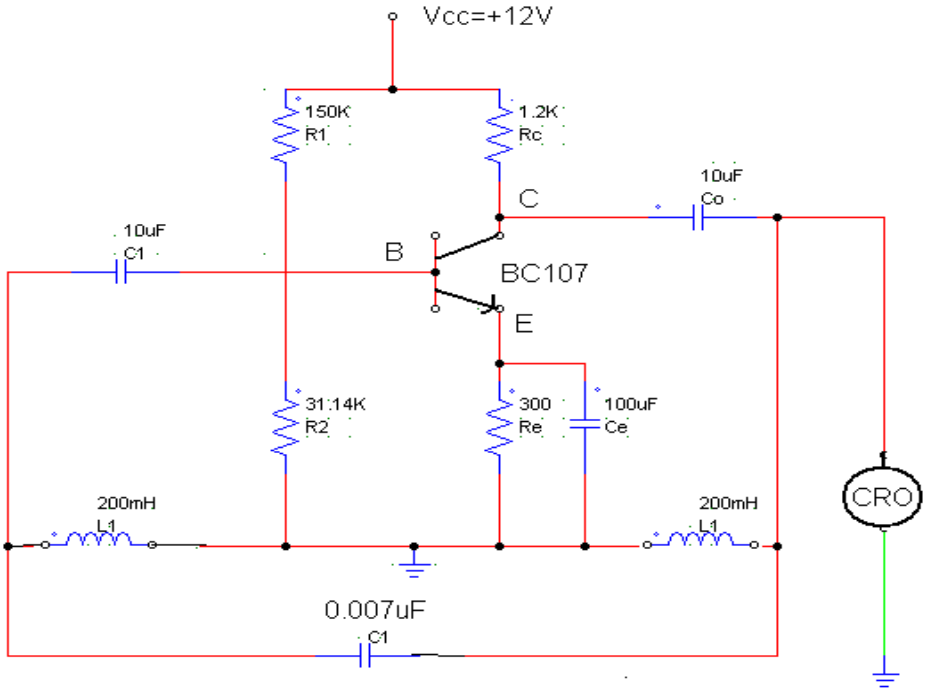
As V_{CE},$I_{C(MAX)}$,$h_{fe(max)}$and $V_{be(sat)}$.

- $V_{CC}= V_{CEQ}+I_{CQ}(R_C+R_E)$
- $R_2=S* R_E$
- $V_{CC}[R_2/(R_1+ R_2)=V_{BE}+V_{BE(SAT)}$
- $V_{R1}+V_{R2}=V_{CC}$

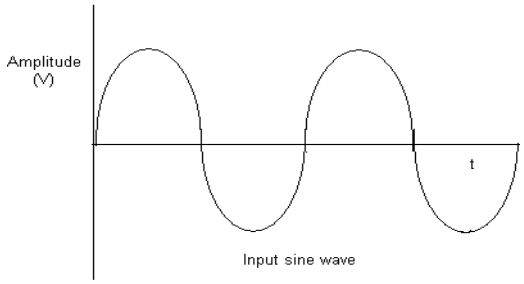
PROCEDURE:

- Hook up the circuit as shown in the circuit diagram.
- Switch on the power supply.
- Slight modification in value of $L_1$and L_2can be made to get perfect sine wave output.
- Observe the output waveform in CRO.

CIRCUITDIAGRAM:HARTLEY OSCILLATOR



MODELGRAPH:



TABULATION:

Amplitude(Volts)	Time(ms)	Frequency(KHz)

RESULT:

Thus the Hartley oscillator wasdesignedand its output waveform was verified.

VIVA QUESTIONS:

1. What arethe types ofsinusoidal oscillator?Mentionthe differenttypes ofsinusoidaloscillator?

RC phase shift Oscillator.Wein bridge Oscillator.
HartleyOscillatorColpitts
OscillatorCrystalOscillator

2. What is Barkhausancriterion?

The conditions foroscillatorto produce oscillation is given byBarkhausancriterion.Theyare:

(i). Thetotal phaseshift producedbythecircuit should be360^oor 0^o(ii).The Magnitudeof loop gain must be greaterthan or equal to 1

i.e.. $A|\omega| \geq 1$.

3. Name two highfrequencyOscillators.

i. HartleyOscillator
ii. ColpittsOscillatoriii.Crystal Oscillator

4. What are the essentialparts of an Oscillator?

i. Tankcircuit(or)Oscillatorycircuit.
ii. Amplifier(Transistoramplifier)
iii. FeedbackCircuit.

Ex No:5(a)

Date:

COLLECTOR COUPLED ASTABLE MULTIVIBRATOR

Aim :-

To design an Astable Multivibrator to generate a Square wave. Choose C = 1nf, 10nf, 100nf.

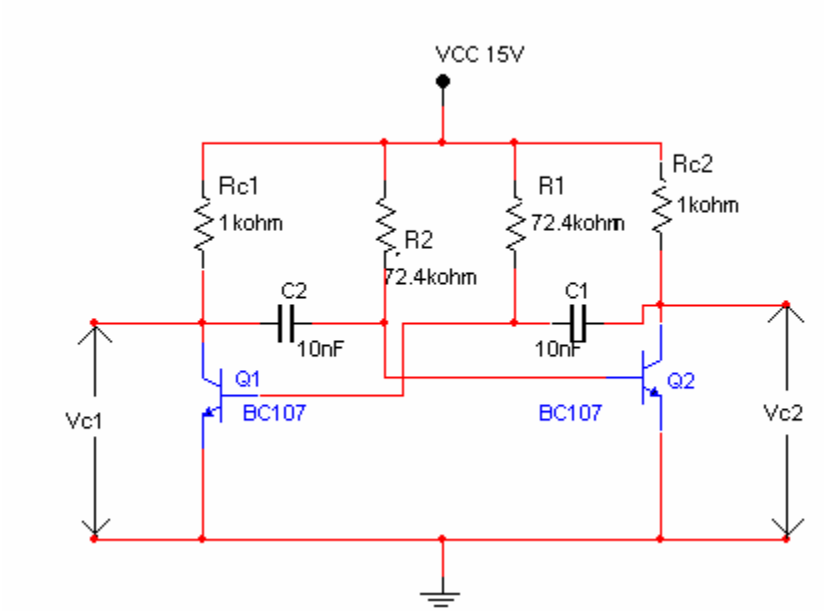
Apparatus:

S.No	Name of the component	Specification	Quantity
1.	Resistors	1kΩ	2
		72.4kΩ,1 kΩ	2,2
2.	Transistor	BC 107	2
3.	Capacitor	10nF	
4.	Bread board	_	1
5.	Connecting wires	_	1 Bunch
6.	CRO	(0-20)MHz	1
7.	Dual Regulated Power supply	(0-30) V DC	1

Theory:

The astable circuit has two quasi-stable states. Without external triggering signal the astable configuration will make successive transitions from one quasi-stable state to the other. The astable circuit is an oscillator. It is also called as free running multivibrator and is used to generate "Square Wave". Since it does not require triggering signal, fast switching is possible.

Circuit diagram:-



Design:

The period T is given by

$T = T1 + T2 = 0.69 (R1C1 + R2C2)$

For symmetrical circuit with R1 = R2 = R & C1 = C2 = C

$T = 1.38 RC$

$10^{-3} = 1.38 \times 10^{-9} \times R$

$R = 72.4K\Omega$ (When c=1nf) ;

$R = (10^{-3}) / 1.38X10X10^{-9}$

$=72.4\ K\ \Omega$ (where c=10nf)

$R=7.24\ K\ \Omega$ (where c=100nf)

Let Vcc=15V ,h_{fe}=51(for BC 107)

Vbe sat=0.7V , Vce sat=0.3 V

Choose Ic max=10 mA

$RC = (V_{CC} - V_{CESat}) / I_{Cmax}$

$= (15 - 0.3) / (10 \times 10\text{-}3) = 1.47K\Omega$

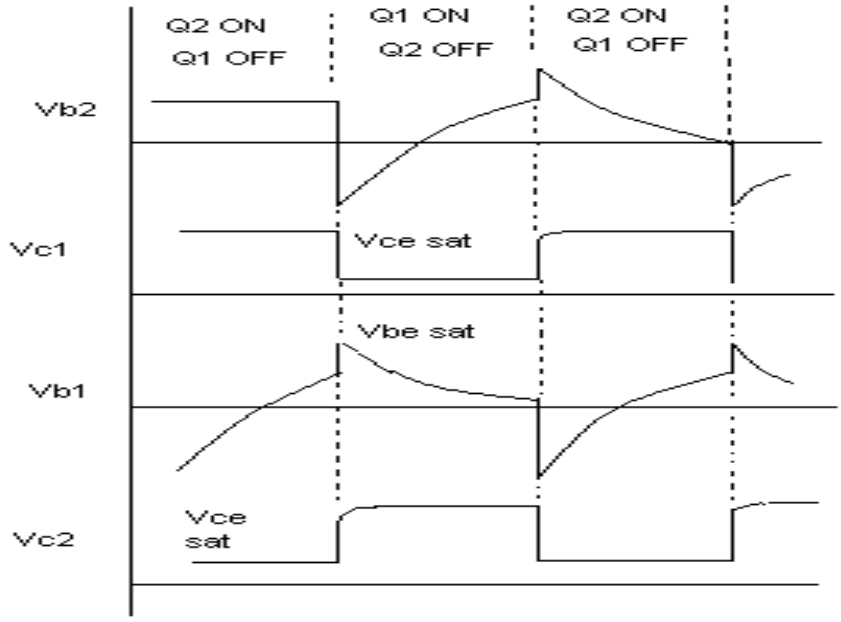
$\therefore\ RC \cong 1K\Omega$

Procedure:

1. Connect the circuit as shown in figure.
2. Apply the supply voltage Vcc =15V
3. Calculate the pulse width (T) of the Astable O/P with the selected values of R & C on the CRO. See that CRO is in DC mode.
4. Connect the CRO channel-1 to the collector and base of the Transistor Q1&Q2..
5. Measure the pulse width and verify with the theoretical value.
6. Obtain waveforms at different points like VB1, VB2, VC1 & VC2.

.

Expected wave forms:-



Tabulation:

Sl No	Amplitude(Volts)	Time(ms)	Frequency

Result : An Astable Multivibrator was designed, the waveforms are observed and verified the results theoretically.

Questions:

1. Is it possible to change time period of the waveform with out changing R & C? Support your answer?
2. Collector waveforms are observed with rounded edges. Explain?
3. Explain charging and discharging of capacitors in an Astable Multivibrator?
4. How can an Astable multivibrator be used as VCO?
5. Why do you get overshoots in the Base waveforms?
6. What are the applications of Astable Multivibrator?
7. How can Astable multivibrator be used as a voltage to frequency converter?
8. What is the formula for frequency of oscillations?
9. What are the other names of Astable multivibrator?

Ex No:5 (b)

Date:

EMITTER COUPLED ASTABLE MULTIVIBRATOR

Aim :-

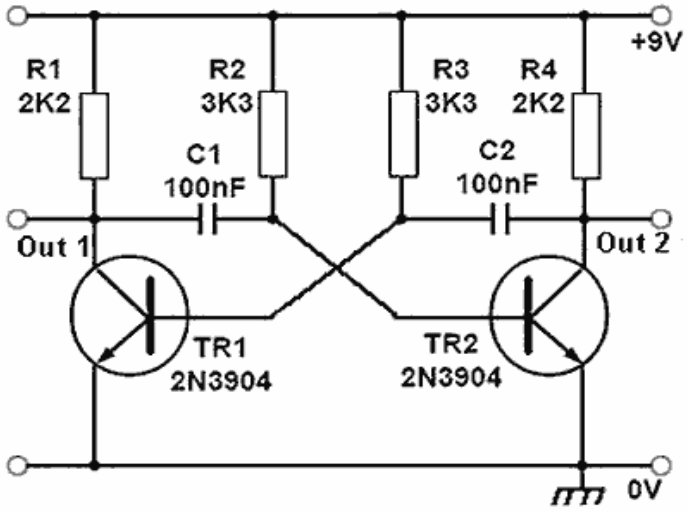
To design an Emitter Coupled Astable Multivibrator to generate a Square wave. Choose C =100nf.
Apparatus:

S.No	Name of the component	Specification	Quantity
1	Resistors	2.2kΩ	2
		3.3 kΩ	2
2.	Capacitor	100nF	
3	Transistor	2N3904	2
4	Bread board	_	1
5	Connecting wires	_	1 Bunch
6	CRO	(0-20)MHz	1
7	Dual Regulated Power supply	(0-30) V DC	1

Theory:

1. In D.C. conduction i.e. with timing capacitor C removed bias should be so adjusted that both the transistors are in active region.
2. Under D.C. condition, the D.C. loop gain should be less than unity to void bistable operation.
3. In the active region, the loop gain must be greater than unity at some non-zero frequency.
4. Bias conditions ar3e so adjusted that with the capacitor C concerned, during normal operation, transistor C_1 operates between cut-off and saturation while transistor C_2 operates at the same time between its active region and the off region. This transistor Q_1 operates in saturated mode and transistor Q_1 operates in saturated mode and transistor Q_2 operates in unsaturated mode.

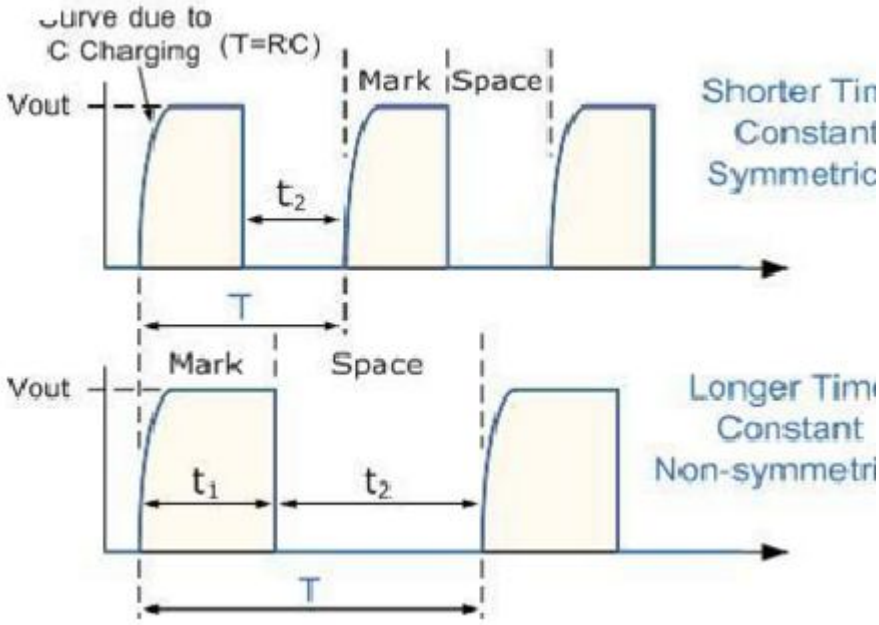
Circuit Diagram:



Procedure:

1. Connect the circuit as shown in figure.
2. Apply the supply voltage Vcc =15V
3. Calculate the pulse width (T) of the Astable O/P with the selected values of R & C on the CRO. See that CRO is in DC mode.
4. Connect the CRO channel-1 to the collector and base of the Transistor Q1&Q2..
5. Measure the pulse width and verify with the theoretical value.
6. Obtain waveforms at different points like VB1, VB2, VC1 & VC2.

Expected wave forms:-



Tabulation:

Sl No	Amplitude(Volts)	Time(ms)	Frequency

Result : An Astable Multivibrator was designed, the waveforms are observed and verified the results theoretically.

Ex No:6

Date:

WEIN BRIDGE OSCILLATOR

AIM:

To design and set up a Wein Bridge oscillator using Transistor and to observe the sinusoidal output waveform.

APPARATUS REQUIRED:

S.NO.	NAME OF THE EQUIPMENT	TYPE	RANGE	QUANTITY (NO.S)
1	Transistor	BC547	-	2
2	Resistors	-	47kΩ, 10kΩ,2.2kΩ,680Ω	one from each
3	Resistor	-	4.7kΩ	3
3	Capacitors	-	1μF,22μF	one from each
4	Capacitor	-	0.01 μF	3
5	CRO	-	(0-20)MHz	1
6	RPS	-	(0 – 30V)	1
7	Bread Board	-	-	1
8	Connecting wires	-	-	Required

THEORY:

An oscillator is an electronic circuit for generating an AC signal voltage with a DC supply as the only input requirement. The frequency of the generated signal is decided by the circuit elements used. An oscillator requires an amplifier, a frequency selective network and a positive feedback from the output to the input.The Barkhausen criterion for sustained oscillation is $A\beta = 1$ where A is the gain of the amplifier and β is the feedback factor (gain).The unity gain means signal is in phase. (If the signal is 180^0 out of phase and gain will be -1).

A Wien bridge oscillator is a type of electronic oscillator that generates sine waves. It can generate a large range of frequencies. The oscillator is based on a bridge circuit originally developed by Max Wien in 1891 for the measurement of impedances. The bridge comprises four resistors and two capacitors. The oscillator can also be viewed as a positive gain amplifier combined with a bandpass filter that provides positive feedback. Automatic gain control, intentional non-linearity and incidental non-linearity limit the output amplitude in various implementations of the oscillator.

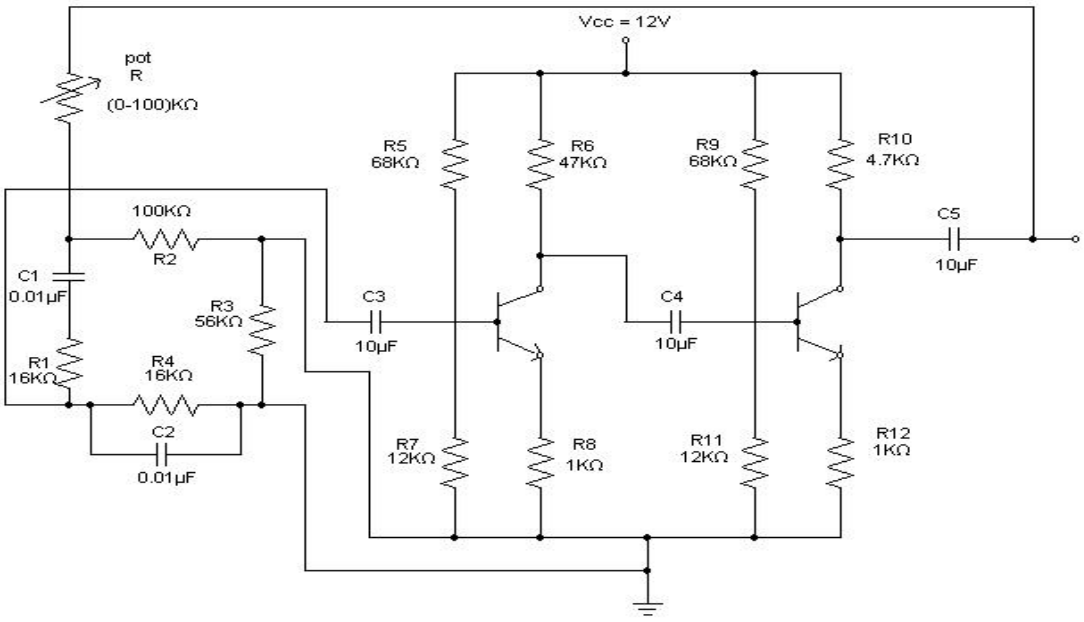
The circuit shown to the right depicts a common implementation of the oscillator, with automatic gain control, using modern components. Under the condition that $R_1=R_2=R$ and $C_1=C_2=C$, the frequency of oscillation is given by:

$$f = \frac{1}{2\pi RC}$$

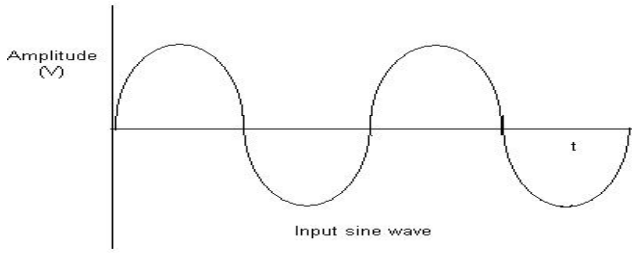
and the condition of stable oscillation is given by

$$R_b = \frac{R_f}{2}$$

CIRCUIT DIAGRAM:



MODEL GRAPH:



PROCEDURE:

1. Identify the pin details of BC107 Transistor (or equivalent silicon Transistor such as BC108/547) and test it using a millimeter. Set up the circuit on breadboard as shown in figure.

2. A 12V Supply Voltage is given by using Regulated power supply and output is taken from collector of the Transistor.
3. By using CRO the output time period and voltage are noted.
4. Plot all the readings curves on a single graph sheet.

Sl No	Amplitude(volts)	Time(ms)	Frequency

RESULT:

Thus the Wein Bridge oscillator using Transistor was obtained and the output waveform was plotted.

Ex No:7

Date:

SCHMITT TRIGGER

Aim:-

To study the operation of Schmitt trigger circuit and find the UTP and LTP voltages & compare with the theoretical values.

Apparatus:

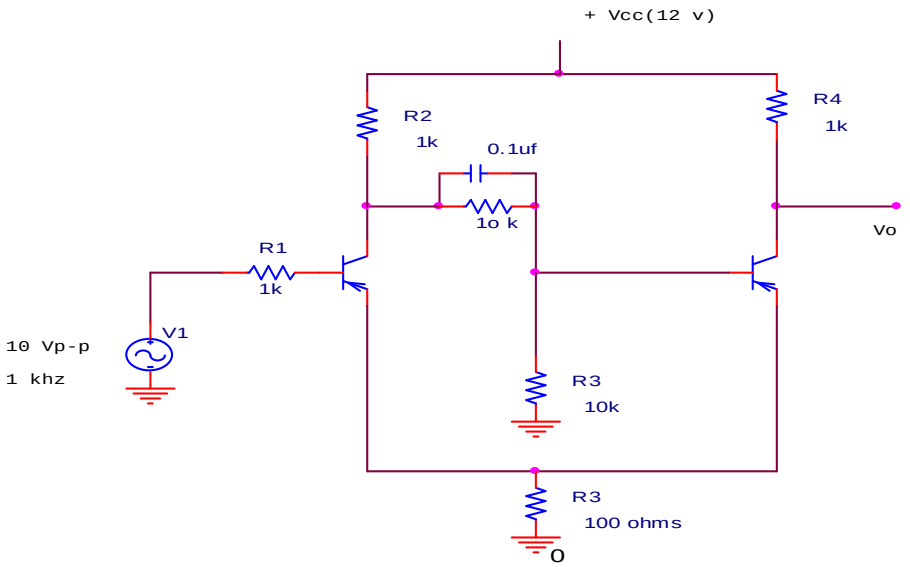
s.no	Name of the component	Specification	Quantity
1.	Transistor	BC107a	2
2.	Resistors	1kΩ 10kΩ 100Ω	2 2 2
4.	Capacitors	0.1uf	1
5.	RPS	(0-30)V	1
6.	Bread board	_	1
7.	Connecting wires	_	-----
8.	Function generator	(0-10)MHz	1
9.	CRO	(0-20)MHz	1

Theory:

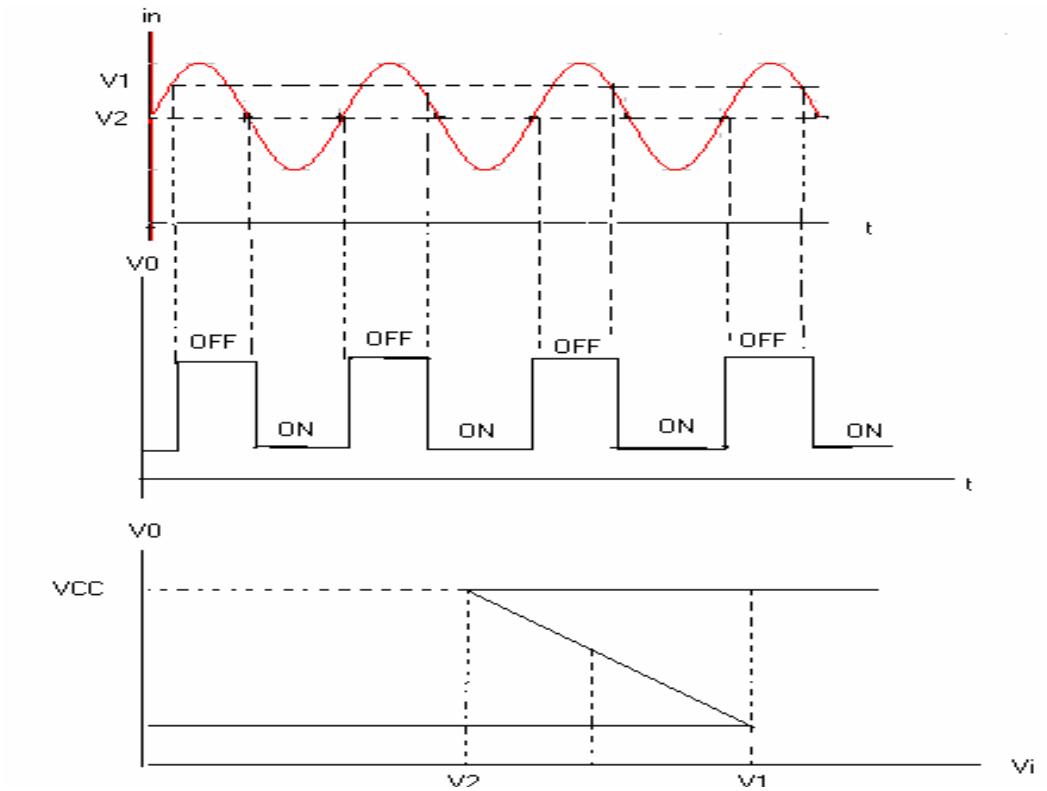
Schmitt trigger is a special type of bistable multivibrator which has several important practical applications. The Schmitt trigger is a emitter coupled binary. Since the emitter of Q_1 and Q_2 are joined and they are grounded through a common resistor R_e. The base of Q_1 is connected to a voltage source V_i. The output is an unsymmetrical square wave. Thus the Schmitt trigger converts the sinusoidal wave to square. It is therefore termed as sine to square wave converter or squaring circuit.

However the output of a Schmitt trigger is a square wave, whatever the waveforms of the input signal. Another application of Schmitt trigger is as a flip-flop.

Circuit diagram :



Expected wave form



Theoretical calculations:

i) Calculation of V_1 [UTP]

$V_1 = V^1\text{-}0.1V$ where $V^1 = (V_{cc}\ R_2)/(RC_1+R_1+R_2)$

$V^1 = (V_{cc}\ R_2)/(RC_1+R_1+R_2)$

=>12x10k / (1k+10k+10k) = 5.714V

$V_1 = UTP = V^1 - 0.1V$

= 5.714V – 0.1V

= 5.61V

ii) Calculation of V_2 [LTP]

$a = R_2/(R_1+ R_2)$

= 10k/(10k+10k) =0.5

$V^1 = aV_T$

=> 0.5x12V =6V (since $V_T = V_{cc}$)

$R = RC_1(R_1+ R_2)/ (RC_1+R_1+R_2)$

= 1k(10k+10k)/(1k+10k+10k)

= 952.38Ω

$V_{BE1} = 0.6V$ & $V_{\gamma 2} = 0.6V$

$V_2 = V_{BE1} + (R_e/aR+ R_e)(V^1 - V_{\gamma 2})$

= 0.6+[100/(0.5x952.38)+100](6-0.6)

= 1.53V

Procedure:

1. Connect the circuit on the bread board as per circuit diagram
2. Keep the peak to peak input voltage 10V using function generator
3. Keep the V_{CC} voltage at 12V constant using regulated power supply
4. Observe the output waveform in the CRO

5. Plot the values and draw the graph

6. Calculate the upper triggering point & lower triggering point

Tabulation:

Sl No	Amplitude(volts)	Time(ms)	Frequency

Questions:

1. What are the applications of Schmitt Trigger?
2. Define hysteresis action?
3. Why is Schmitt Trigger called a squaring circuit?
4. What is UTP?
5. What is LTP?
6. What is the difference between a Binary and Schmitt Trigger?

Result:

The operation of Schmitt trigger is verified and the UTP & LTP voltages in both theoretically and practically compared and verified

Ex No: 8

Date:

BISTABLE MULTIVIBRATOR

Aim:

a) Design the Bi-stable Multivibrator circuit and verify the operation.

b) Obtain the resolving time of Bi-stable Multivibrator and verify theoretically

Choose R_1 = 10KΩ, C = 0.3μf, $V_{ce(sat)}$ = 0.2V, IC_{max} = 15mA, V_{CC} = 15V, V_{BB} = 15V, V_{B1} = -1.2V

Apparatus:

s.no	Name of the component	Specification	Quantity
1.	Transistor	BC107b	2
2.	Diode	IN4007	3
3.	Resistors	1kΩ 10kΩ 100kΩ	5 2 2
4.	Capacitors	0.33uf 0.001uf	3 2
5.	RPS	(0-30)V	1
6.	Bread board	_	1
7.	Connecting wires	_	---
8.	CRO	(0-20)MHz	1

Theory:

A Bistable circuit is one which can exist indefinitely in either of two stable states and which can be induced to make an abrupt transition from one state to the other by means of external excitation. The Bistable circuit is also called as Bistable multivibrator, Eccles jordon circuit, Trigger circuit, Scale-of-2 toggle circuit, Flip-Flop & Binary.

A bistable multivibratior is used in a many digital operations such as counting and the storing of binary information. It is also used in the generation and processing of pulse-type waveform. They can be used to control digital circuits and as frequency dividers .

There are two outputs available which are complements of one another. i.e. when one output is high the other is low and vice versa .

Design :

$R_c = [V_{cc} – V_{ce\ (sat)}\ ] / I_{c(max)}$

RC = (15 – 0.2) / 15mA ≈ 1KΩ

Choose RC = 1KΩ, VB1 = $(-V_{bb}\, R_1 / R_1 + R_2) / (V_{ce\ (sat)}\, R_2 / R_1 + R_2)$

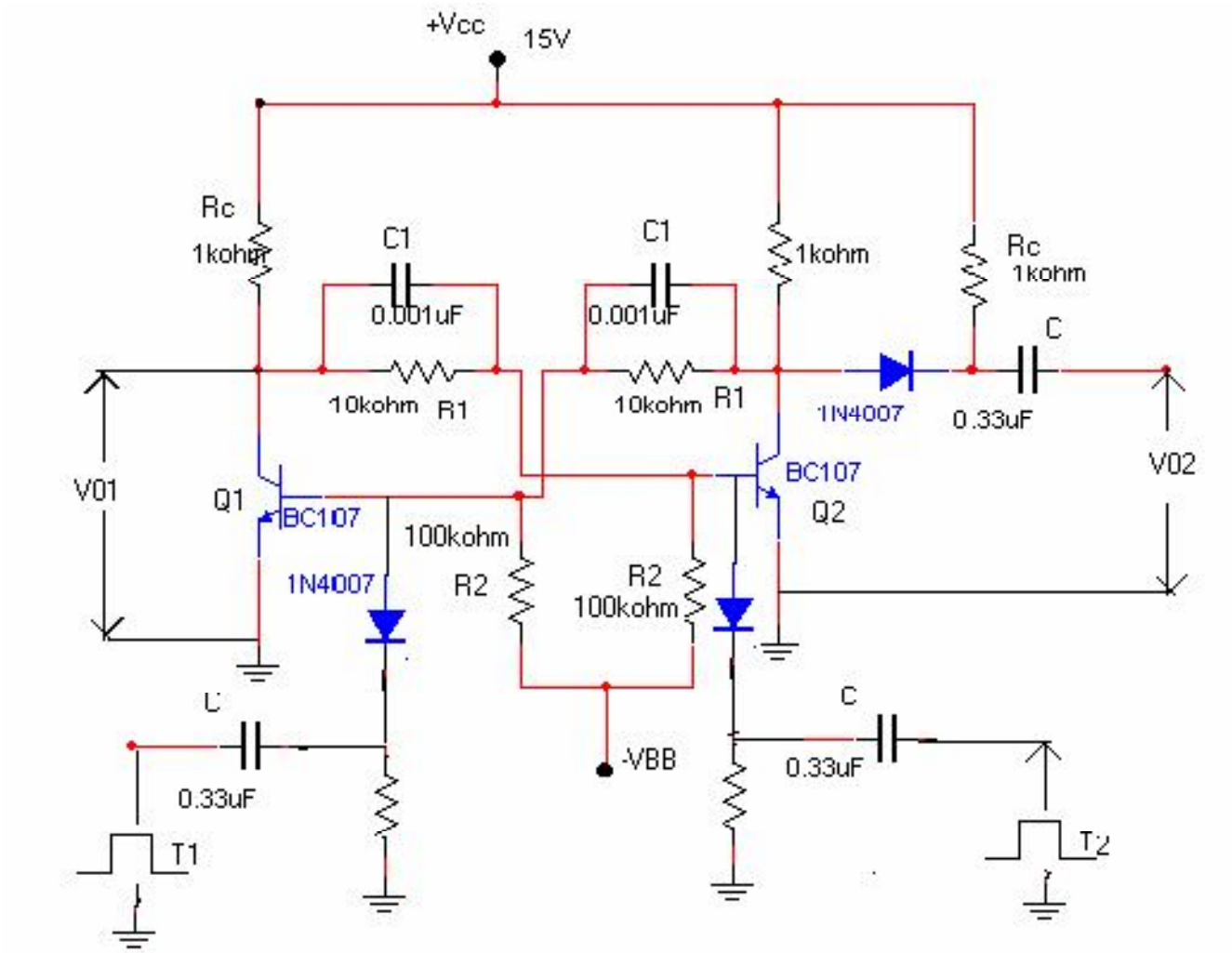
$-1.2 = (-15x10+0.2R_2)/(10+ R_2)$; $R_2 = 100k\Omega$

$f_{max} = (R_1+R_2)/2CR_1R_2$

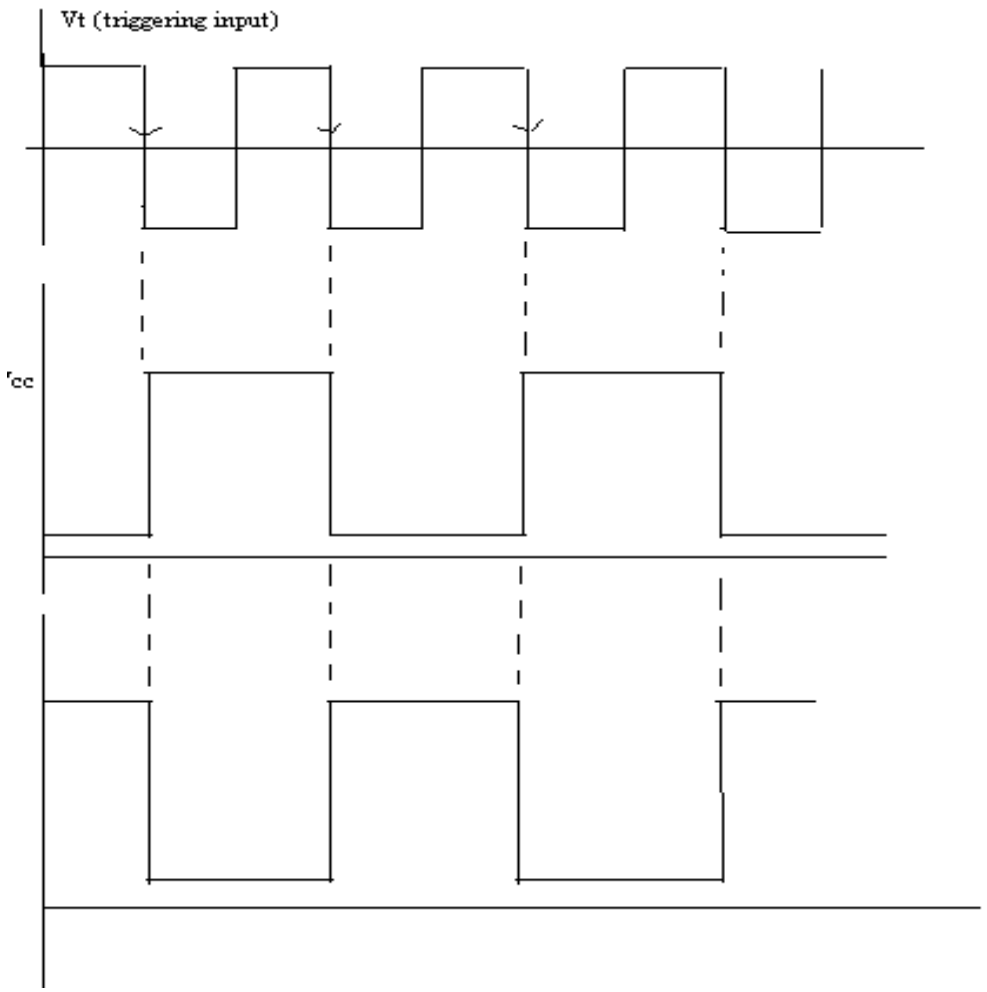
$= (10+100k)/(2x0.3x10^{-6}x10kx100k)$

= 55khz

Circuit diagram:



Expected waveforms:



Procedure:

1. Check the square wave output from CRO to conform the voltage is $0.5V_{pp}$.
2. Connect the circuit as shown in the circuit diagram
3. Apply sine wave as input at the transistor Q_1 across collector and emitter terminals
4. Check whether the output waveform at the transistor Q_2 is square wave or not
5. Measure the amplitude of output wave form and check whether the loop gain is less than 1
6. Similarly apply the input at transistor Q_2
7. Repeat the steps 3 and 4 and note down the amplitude and output waveform

Tabulation:

Sl No	Amplitude(volts)	Time(ms)	Frequency

Result:

Bistable Multivibrator circuit is designed and output waveforms are observed

Questions: -

1. What are the applications of a Bitable multivibrator?
2. Describe the operation of commutating capacitors?
3. Why is a Binary also called a flip-flop?
4. Mention the name of different kinds of triggering used in the circuit shown?
5. What are the disadvantages of direct coupled Binary?
6. How many types of unsymmetrical triggering are there?

Ex No:9

Date:

MONOSTABLE MULTIVIBRATOR

Aim : To design a monostable multivibrator for the Pulse width of 0.03mSec.

Apparatus:

S.No	Name of the component	Specification	Quantity
1.	Resistors	1kΩ	2
		10kΩ	2
		43.2kΩ	2
		100kΩ	1
2.	Transistor	BC 107	2
3.	Capacitor	0.047µF,10nF	2,1
4.	Diode	In4007	1
5.	Trainer kit	_	1
6.	Connecting wires		1 Bunch
7.	CRO		1
8.	Dual Regulated Power supply	(0-30) V DC	1

Theory:

The monostable circuit has one permanently stable and one quasi-stable state. In the monostable configuration, a triggering signal is required to induce a transition from the stable state to the quasi-stable state. The circuit remains in its quasi-stable for a time equal to RC time constant of the circuit. It returns from the quasi-stable state to its stable state without any external triggering pulse. It is also called as one-shot a single cycle, a single step circuit or a univibrator.

Design:-

To design a monostable multivibrator for the Pulse width of 0.03mSec.

Choose ICmax = 15mA, VCC = 15V, VBB = 15V, R1 = 10KΩ.

$T = RC \ln 2$

$T = 0.69\ RC$ Choose $C = 10nf$

$0.3 \times 10^{-3}Sec = 0.69 \times R \times 10 \times 10^{-9}$

$R = 43.47\ K\Omega.$

$Rc = (Vcc - Vce\ sat)/ Ic\ max.$

$RC = (15 - 0.2) / 15mA \approx 1K\Omega$

For more margin Given,

VB1= -1.185

$$VB1= \frac{-V_{BB}\, R_1}{R1+R2} + \frac{Vce\ sat\ R_2}{R1+R2}$$

-1.18=(-15 R1+ 0.2 R2) / (R1+R2)

Given R1=10 KΩ

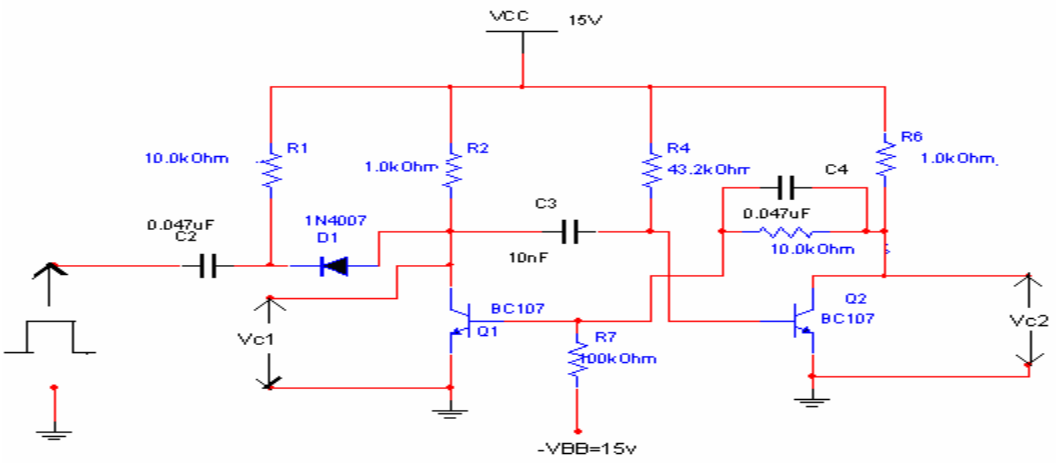
We will R2= 100K

Procedure:

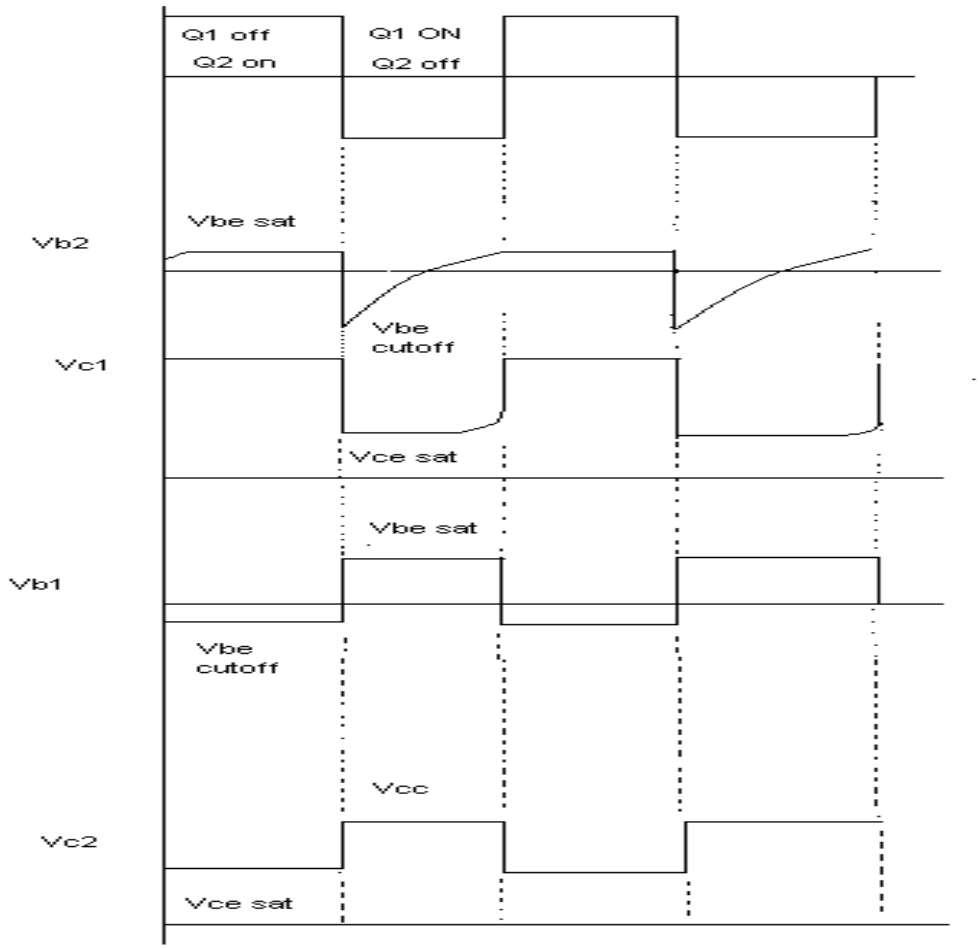
1. Wire the circuit as shown in the circuit diagram.
2. Calculate the pulse width (T) of the Monostable O/P with the selected values of R & C on the CRO. See that CRO is in DC mode.
3. Select the triggering pulse such that the frequency is less than 1/T
4. Apply the triggering input to the circuit and to the CRO's channel 1 . Connect the CRO channei-2 to the collector and base of the TransisterQ1&Q2..
5. Adjust the triggering pulse frequency to get stable pulse on the CRO and now measure the pulse width and verify with the theoretical value.
6. Obtain waveforms at different points like VB1, VB2, VC1 & VC2.
7. Repeat the experiment for different combinations of R & C (C = 1nf, 100nf).

Calculate R for same value of T = 0.3 mSec.

Circuit Diagram:-



Expected wave forms:-



Tabulation:

Sl No	Amplitude(volts)	Time(ms)	Frequency

Result :

A collector coupled Monostable Multivinbrator is designed, the waveforms are observed and verified the results theoretically.

Ex No:9

Date:

CLASS C TUNED AMPLIFIER

Aim: To design the characteristics of Class C Tuned Amplifier

Apparatus:

Sl No	Component	Range	Quantity
1	Transistor	SL100	1
2	Resistor	10 kΩ,200Ω	2,1
3	Capacitor	0.01mf,0.10µf	1
4	Inductor	1mH	1
5	RPS	(0-30)V	1
6	CRO	(0-20)MHz	1
7	Function generator	(0-10)MHz	1
8	Connecting wires	-	Bunch
9	Bread board	-	1

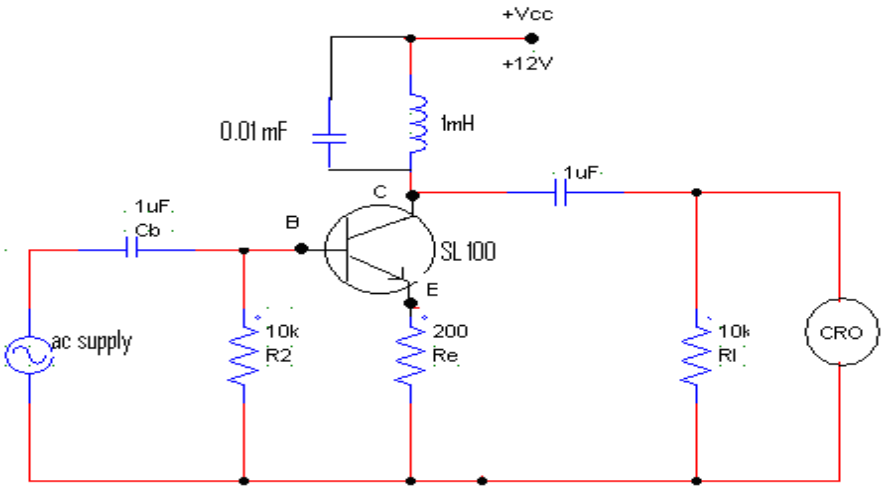
THEORY:

The amplifier is said to be class c amplifier if the Q Point and the input signal are selected such that the output signal is obtained for less than a half cycle, for a full input cycle Due to such a selection of the Q point, transistor remains active for less than a half cycle .Hence only that much Part is reproduced at the output for remaining cycle of the input cycle the transistor remains cut off and no signal is produced at the output .the total Angle during which current flows is less than 180°.This angle is called the conduction angle, Qc

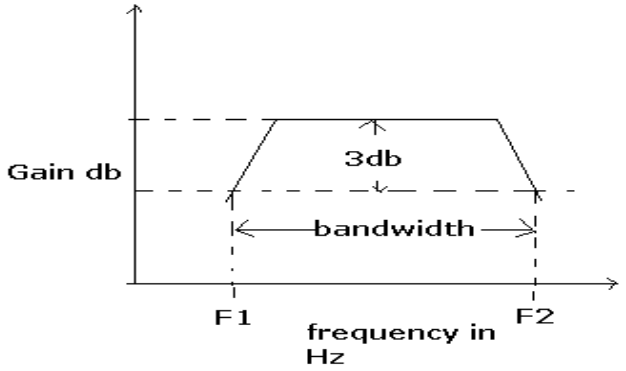
PROCEDURE:

1.The connections are given as per the circuit diagram.
2. Connect the CRO in the output and trace the waveform.
3.calculate the practical frequency and compare with the theoretical Frequency
4.plot the waveform obtained and calculate the bandwidth

CIRCUIT DIAGRAM:



MODEL GRAPH



TABULATION:

Sl. No.	Inputfrequency(Hz)	InputVoltage(mV)	Output Voltage (V)	Voltagegain $V_{gain} = 20\log\left(\frac{V_o}{V_i}\right)$ db

Result:

Thus a class C amplifier was designed and waveforms are observed and verified.

SIMULATION USING PSPICE

EXP.NO: 11
DATE:

FREQUENCY RESPONSEOF CE AMPLIFIER WITH EMITTER RESISTANCE.

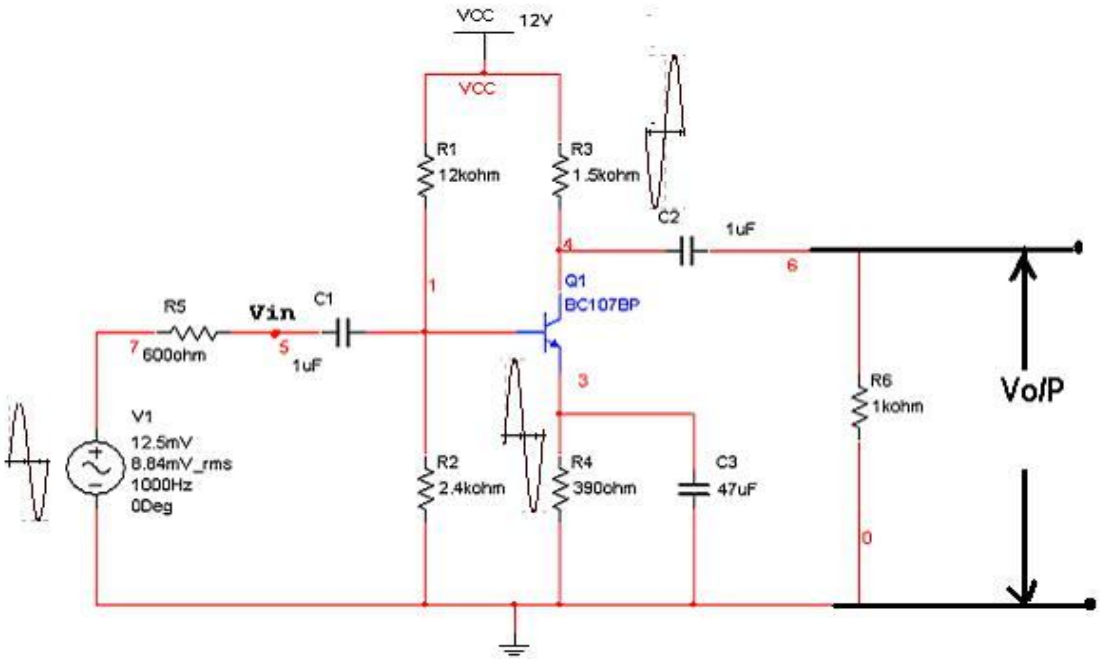
AIM :

To design and simulate the frequency response of common emitter amplifier for a gain of 50.

APPARATUS REQUIRED:

- PC with SPICE software

CIRCUIT DIAGRAM :



THEORY:

The CE amplifier provides high gain and wide frequency response. The emitter lead is common to both the input and output circuits are grounded. The emitter base junction is at forward biased .The collector current is controlled by the base current rather than the emitter current. The input signal is applied to the base terminal of the transistor and amplified output taken across collector terminal. A very small change in base current produces a much larger change in collector current. When the positive is fed to input circuit it opposes forward bias of the circuit which cause the collector current to decrease, it decreases the more negative. Thus when input cycle varies

through a negative half cycle, increases the forward bias of the circuit, which causes the collector current increases .Thus the output signal in CE is out of phase with the input signal.

PROCEDURE

1. Select different components and place them in the grid.
2. For calculating the voltage gain the input voltage of 25mv (p-p) amplitude and 1KHz frequency is applied, then the circuit is simulated and output voltage is noted.
3. The voltage gain is calculated by using the expression

   $$Av = Vo/Vi$$

4. For plotting frequency response, the input voltage is kept constant at 25mv(p-p) and frequency is varied.
5. Note down the output voltage for each frequency.
6. All readings are tabulated and Av in db is calculated using the formula

   $$20 \text{ og } Vo/Vi.$$

7. A graph is drawn by taking frequency on X-axis and gain in dB on Y-axis on a Semi log graph sheet.

SPICE FILE :

```
VIN 1 4 SIN(0 1.5V 2KHZ)
VB 4 0 2.3V
RL 3 0 15K
V1 2 0 15V
Q1 2 1 3 MOD1
.MODEL MOD1 NPN
.TRAN 0.02MS 0.78MS
.PROBE
.END
```

THEORITICAL CALCULATIONS :

$$V_B = \frac{R_2}{R_1 + R_2} \times V_{CC} = \frac{2400}{14400} \times 12 = 2V$$

$$V_E = V_B - V_{BE} = 2 - 0.7 = 1.3V$$

$$IE = \frac{VE}{RE} = \frac{1.3}{390} = 3.3mA$$

$$V_C = V_{CC} - I_C \times R_C = 12 - 0.0033 \times 1500 = 7.05V$$

To calculate A_V, $Z_{in(base)}$ and Z_{in} :

$$r'_e = \frac{25mV}{I_E} = \frac{25}{3.3} = 7.575\Omega$$

$$r_L = \frac{R_C \times R_L}{R_C + R_L} = \frac{1500 \times 1000}{1500 + 1000} = 600\Omega$$

$$A_V = \frac{r_L}{r'_e} = \frac{600}{7.575} = 79.20$$

$$Z_{in(base)} = \beta r'_e = 40 \times 7.575 = 303\Omega$$

$$Z_{in} = Z_{in(base)} \parallel R_1 \parallel R_2 = 303 \parallel 12000 \parallel 2400 = 263\Omega$$

$$V_b = \frac{Z_{in}}{R_G + Z_{in}} \times 25mV = \frac{263}{600 + 263} = 7.61mV$$

$$V_{out} = A_V \times V_b = 79.20 \times 7.61mV = 0.603V$$

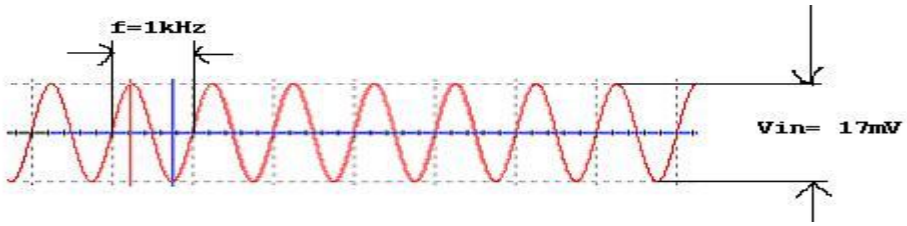
PRACTICAL CALCULATIONS :

$$V_{in} =$$

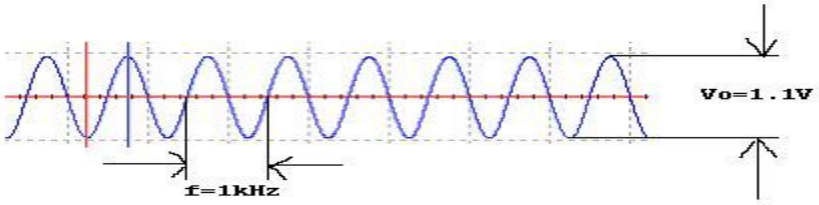
$$V_{out} =$$

$$A_V = \frac{V_{out}}{V_{in}} =$$

INPUT WAVE FORM :



OUT PUT WAVE FORM :



RESULT:

Thus the simulation of class-B amplifier using PSPICE was simulated successfully.

EXP.NO: 12

DATE:

DC RESPONSEOF CS AMPLIFIER

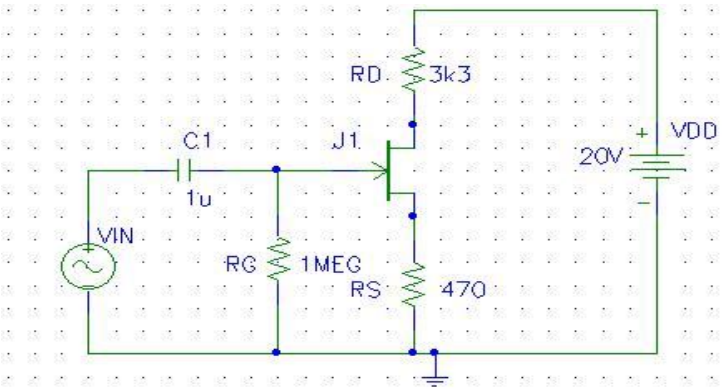
AIM:

To find the DC response of CS amplifier.

APPARATUS REQUIRED:

- PC with SPICE software

CIRCUIT DIAGRAM:



THEORY:

In electronics, a **common-source** amplifier is one of three basic single-stage field-effect transistor (FET) amplifier topologies, typically used as a voltage or transconductance amplifier. The easiest way to tell if a FET is common source, common drain, or common gate is to examine where the signal enters and leaves. The remaining terminal is what is known as "common". In this example, the signal enters the gate, and exits the drain. The only terminal remaining is the source. This is a common-source FET circuit. The analogous bipolar junction transistor circuit is the common-emitter amplifier.

The common-source (CS) amplifier may be viewed as a transconductance amplifier or as a voltage amplifier. (See classification of amplifiers). As a transconductance amplifier, the input voltage is seen as modulating the current going to the load. As a voltage amplifier, input voltage modulates the amount of current flowing through the FET, changing the voltage across the output resistance according to Ohm's law. However, the FET device's output resistance typically is not high enough for a reasonable transconductance amplifier (ideally infinite), nor low enough for a decent voltage amplifier (ideally zero). Another major drawback is the

amplifier's limited high-frequency response. Therefore, in practice the output often is routed through either a voltage follower (common-drain or CD stage), or a current follower (common-gate or CG stage), to obtain more favourable output and frequency characteristics. The CS–CG combination is called a cascode amplifier.

PROCEDURE:

1.Measure the DC operating point of each transistor and compare your results with the calculated values.

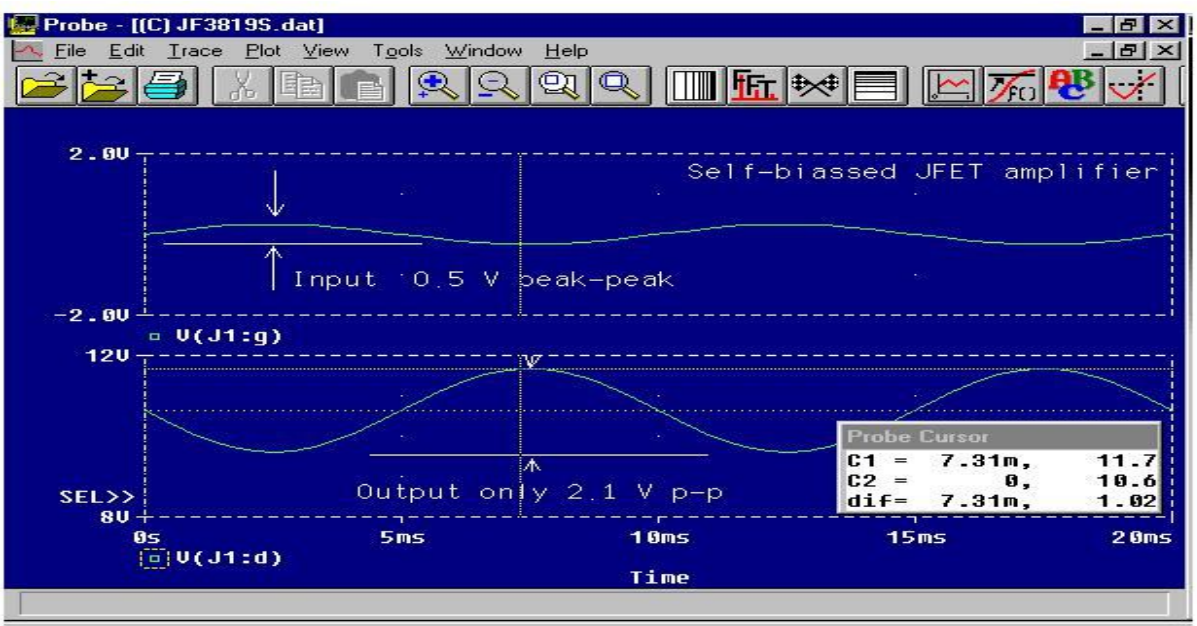
2.At a frequency of 5 KHz, measure the voltage gain, the input and the output resistance and compare your results withthe theoretical values. Calculate the power gain from both experimental and theoretical values.

3.Find the maximum peak-to-peak output voltage swing (i.e. the maximum swing without distortion).

4.Measure the frequency response of the circuit and comment on the change observed in comparison with a single stage common-emitter amplifier.

5.Simulate the circuit using Pspice. Compare the Pspice results with those obtained in the previous parts.

OUTPUT WAVEFORM:



RESULT:

Thus the simulation of DC response of CS amplifier was simulatdd successfully.

EXP.NO: 13

DATE:

FREQUENCY RESPONSEOF CASCODE AMPLIFIER

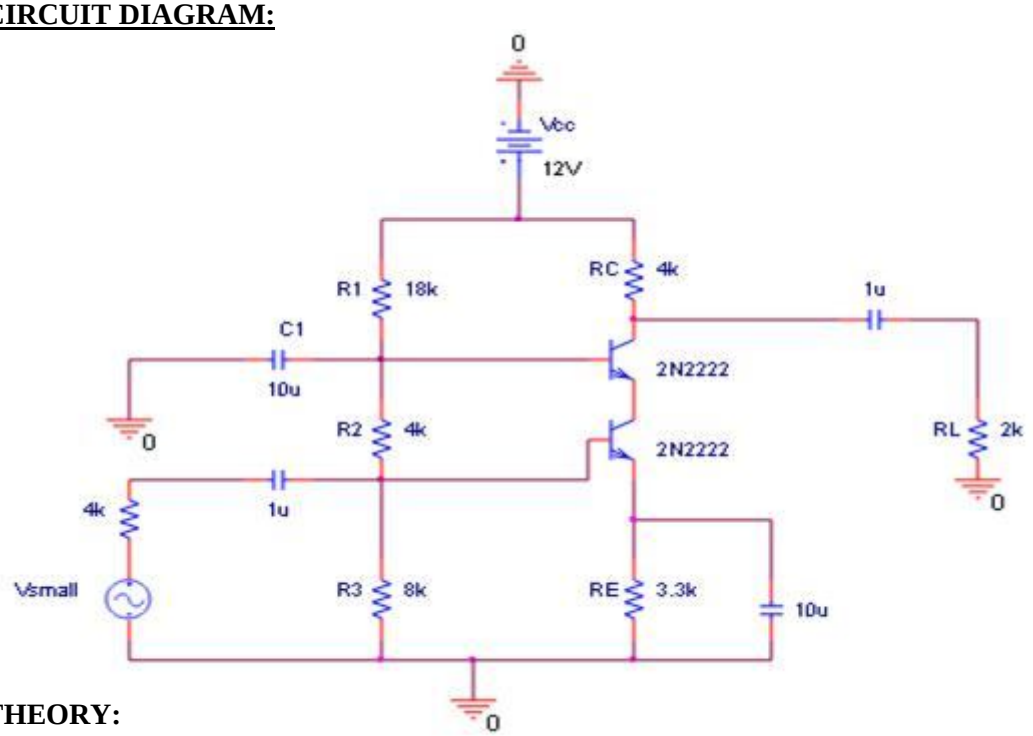
AIM:

To determine the frequency response of Cascode Amplifier.

APPARATUS REQUIRED:

- PC with SPICE software

CIRCUIT DIAGRAM:



THEORY:

Cascode amplifier is a two stage circuit consisting of a transconductance amplifier followed by a buffer amplifier. The word “cascode” was originated from the phrase “cascade to cathode”. This circuit have a lot of advantages over the single stage amplifier like, better input output isolation, better gain, improved bandwidth, higher input impedance, higher output impedance, better stability, higher slew rate etc. The reason behind the increase in bandwidth is the reduction of Miller effect. Cascode amplifier is generally constructed using FET (field effect transistor) or BJT (bipolar junction transistor). One stage will be usually wired in common source/common emitter mode and the other stage will be wired in common base/ common emitter mode.

Miller effect:

Miller effect is actually the multiplication of the drain to source stray capacitance by the voltage gain. The drain to source stray capacitance always reduces the bandwidth and when it gets multiplied by the voltage gain the situation is made further worse. Mulitiplication of stray capacitance increases the effective input capacitance and as we know, for an amplifier, the increase in input capacitance increases the lower cut of frequency and that means reduced bandwidth. Miller effect can be reduced by adding a current buffer stage at the output of the amplifier or by adding a voltage buffer stage before the input.

PROCEDURE:

1.Measure the DC operating point of each transistor and compare your results with the calculated values.

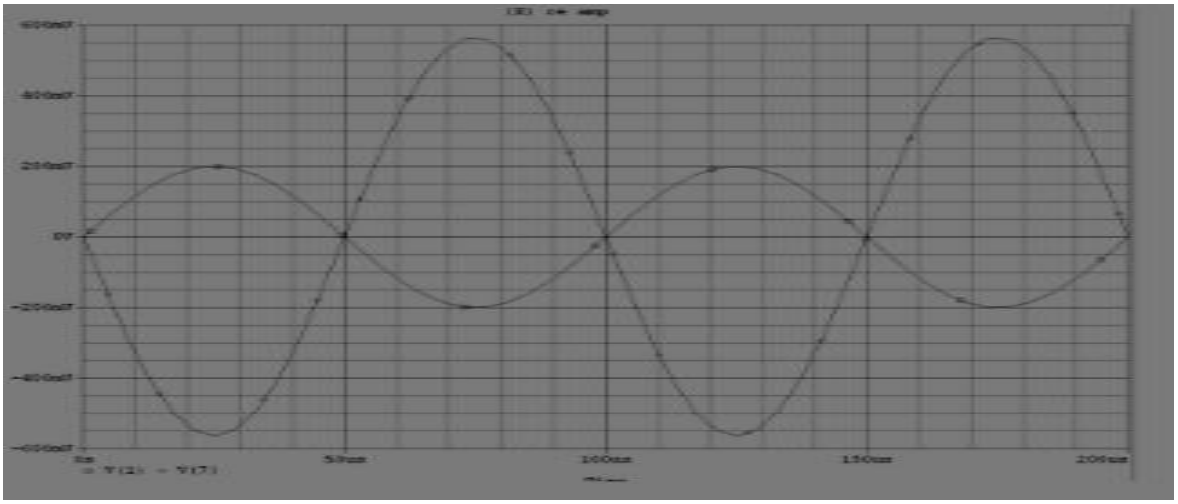
2.At a frequency of 5 KHz, measure the voltage gain, the input and the output resistance and compare your results withthe theoretical values. Calculate the power gain from both experimental and theoretical values.

3.Find the maximum peak-to-peak output voltage swing (i.e. the maximum swing without distortion).

4.Measure the frequency response of the circuit and comment on the change observed in comparison with a single stage common-emitter amplifier.

5.Simulate the circuit using Pspice. Compare the Pspice results with those obtained in the previous parts.

MODEL GRAPH



RESULT:

Thus she simulation of frequency response of Cascode Amplifier was simulated**.**

Ex No:14

Date:

TRANSFER CHARACTERISTICS OF CLASS B POWER AMPLIFIER

AIM:

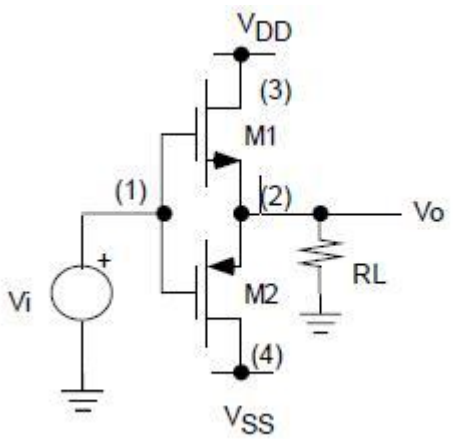
To simulate the Class-B amplifier by using PSICE.

APPARATUS REQUIRED:

- PC with SPICE software

CIRCUIT DIAGRAM:

Class B Amplifier



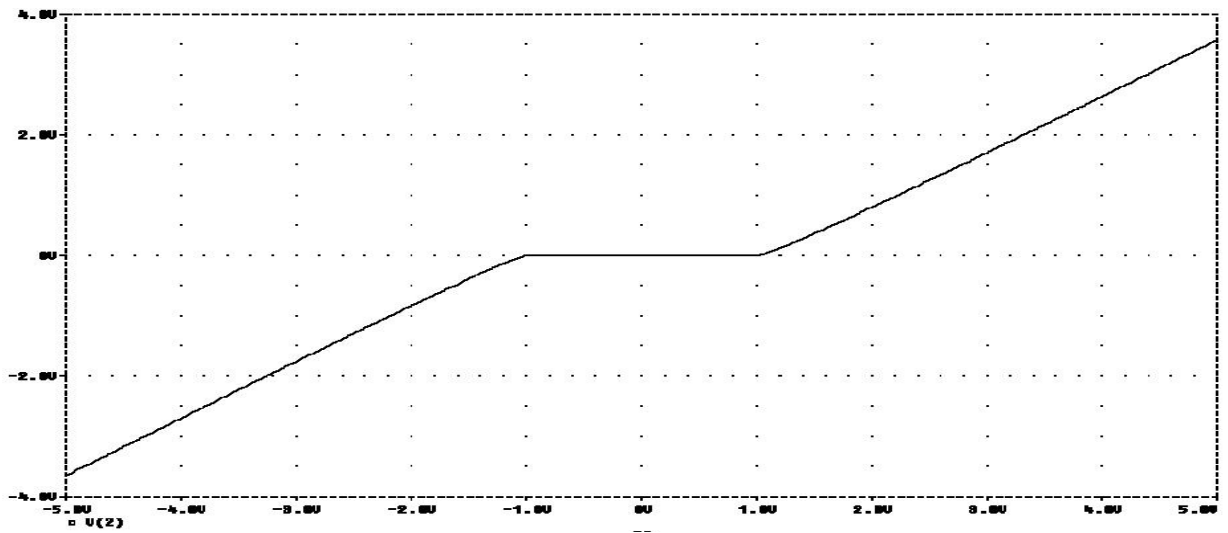
THEORY:

Class-B amplifiers improve the efficiency of the output stage by eliminating quiescent power dissipation by operating at zero quiescent current. This is implemented in Figure 2. As the input voltage V swings positive, M1 turns on when V exceeds the threshold voltage , and the output voltage follows the input on the positive swing. When the input voltage swings negative, M2 turns on when is less than threshold voltage , and the output voltage follows the input on the negative swing. There is a “dead zone” in the class-B voltage transfer characteristic, where both transistors are not conducting.

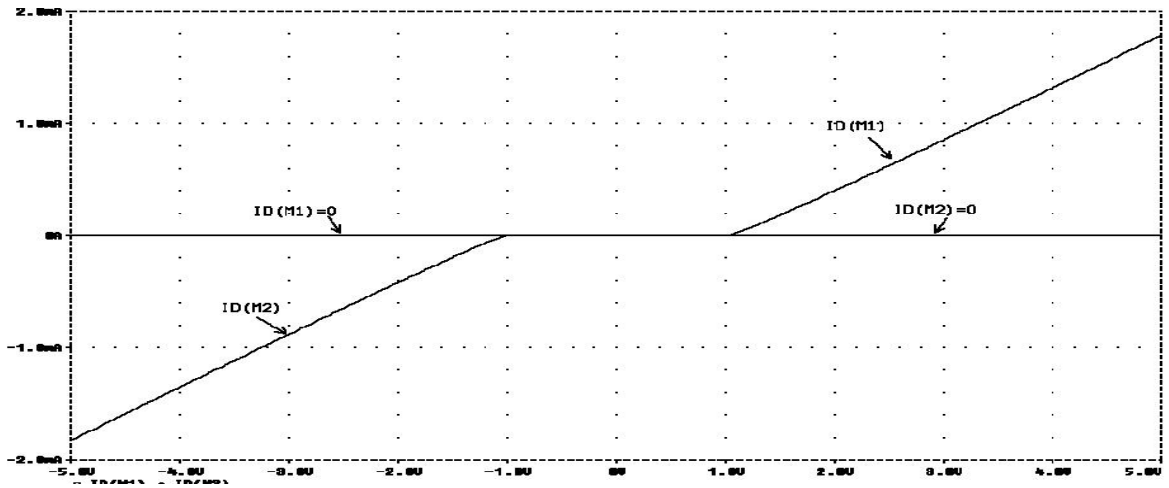
The class-B amplifier is simulated the netlist is shown
below: * Class B Amplifier
*Filename=”classb.cir”

```
VI 1 0 DC 0 sin(0 5 1000)
VDD 3 0 DC 5
VSS 4 0 DC -5
M1 3 1 2 4 N1 W=1000U L=2U
M2 4 1 2 3 P1 W=4000U L=2U RL 2
0 2K
.MODEL N1 NMOS VTO=1 KP=40U
.MODEL P1 PMOS VTO=-1 KP=15U
.OP
.DC VI -5 5 .05
.TF V(2) VI
.TRAN 1U 2M
.PROBE
.END
```

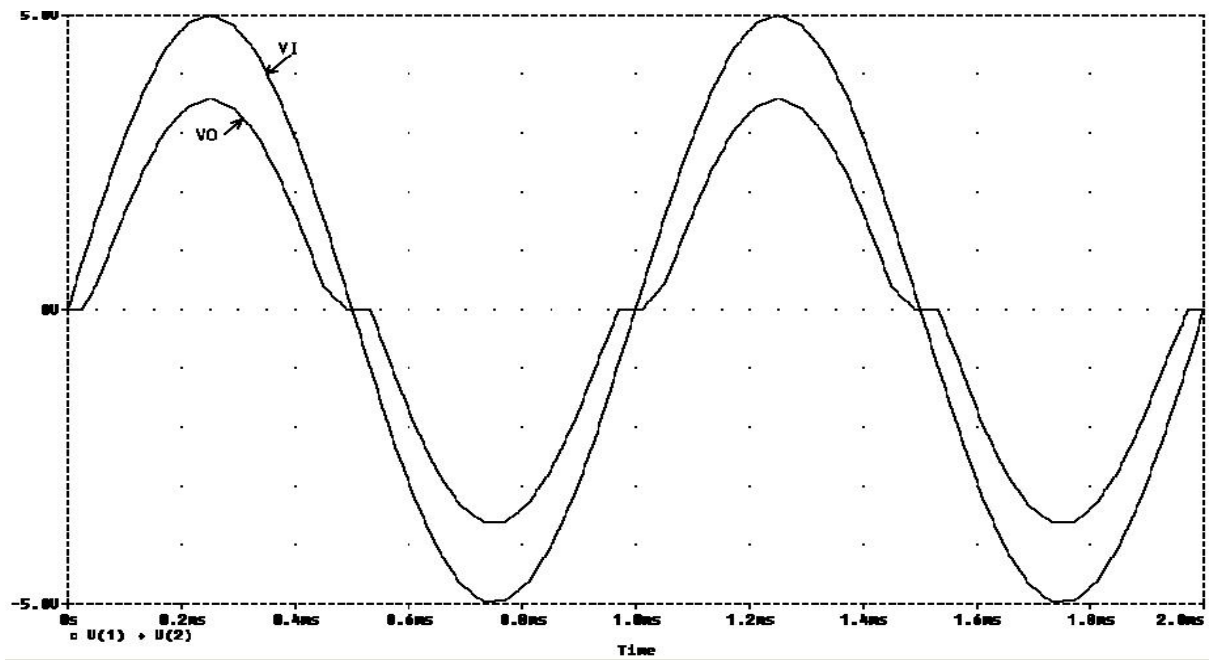
The Pspice simulation shows the presence of the dead zone in the output voltage transfer characteristic.



The current in each transistor conducts for less than half cycle. M1 conducts in the positive half cycle and M2 in the negative half cycle.



The transient analysis shows that the dead zone causes a distortion in the output waveform.



RESULT:

Thus the simulation of class-B amplifier using PSPICE was simulated successfully.